CLAIMS

1. A process for manufacturing an array of cells, comprising the steps of:

providing a body of semiconductor material of a first conductivity type;

implanting, in said body, a common conduction region of said first conductivity type;

forming, in said body, above said common conduction region, a plurality of active area regions of a second conductivity type and a first doping level;

forming, on top of said body, an insulating layer having first and second openings;

implanting first portions of said active area regions through said first openings with a doping agent of said first conductivity type, thereby forming, in said active area regions, second conduction regions of said first conductivity type;

implanting second portions of said active area regions through said second openings with a doping agent of said second conductivity type, thereby forming control contact regions of said second conductivity type and a second doping level, higher than said first doping level, each said control contact region forming, together with said second conduction region and said common conduction region, a selection bipolar transistor; and

forming, on top of said body, a plurality of storage components, each storage component having a terminal connected to a respective second conduction region and defining, together with said bipolar transistor, a cell of said cell array.

2. A process according to claim 1 wherein said step of forming a plurality of active area regions comprises:

forming insulating regions in said body, said insulating regions surrounding said active area regions;

and implanting arsenic in said active area regions.

3. A process according to claim 2 wherein said step of implanting arsenic comprises implanting at an energy of 150-300 keV, preferably about 200 keV, so that said first doping level is between $5*10^{17}$ and $5*10^{18}$ atoms/cm^3.

4. A process according to claim 1 wherein said step of providing a body comprises growing an epitaxial layer of said first conductivity type and a third doping level on a substrate of said first conductivity type and a fourth doping level higher than said third doping level,

the process further comprising, before said step of forming a plurality of active area regions the steps of:

in said epitaxial layer on top of said substrate, implanting a subcollector region of said first conductivity type and a fifth doping level, higher than said third doping level; and

in said epitaxial layer on top of said subcollector region, implanting said common conduction region so that said common conduction region has a sixth doping level, higher than said third doping level and lower than said fifth doping level.

5. A process according to claim 4 wherein said step of implanting the subcollector region comprises implanting 10^{13} to 10^{14} atoms/cm^2 and said fifth doping level is comprised between 10^{17} and 10^{19} atoms/cm^3.

6. A process according to claim 4 wherein said subcollector region is arranged at a depth comprised between 400 and 800 nm.

7. A process according to claim 4 wherein said sixth doping level is comprised between 10^{17} and 10^{18} atoms/cm^3.

8. A process according to claim 7 wherein said subcollector region is arranged at a depth comprised between 200 and 400 nm from a surface of said body.

9. A process according to claim 1 wherein said step of implanting second portions of said active area regions comprises implanting boron at energy in the range of 1 KeV.

10. A process according to claim 9 wherein said second conduction regions extend from a surface of said body to a depth of about 50 nm and have a doping level comprised between 10^{18} and 10^{20} atoms/cm^3.

11. A process according to any claim 1 wherein, before or after implanting said second conduction regions, enriched regions having said second conductivity type are implanted through said first openings to extend below said second conduction regions, said enriched regions having a third doping level higher than said first doping level.

12. A cell array (1) comprising a plurality of cells, each cell including a selection bipolar transistor and a storage component, each said selection bipolar transistor having a first, a second and a control region, and each said storage component having a first and a second terminal, said first region of each bipolar transistor being connected to said first terminal of a respective one of the storage components, said cell array comprising a body of semiconductor material including:

a common conduction region of a first conductivity type, forming said second regions of said selection bipolar transistors;

a plurality of active area regions of a second conductivity type and a first doping level, overlying said common conduction region and forming said control regions of said selection bipolar transistors;

a plurality of second conduction regions of said first conductivity type formed in said active area regions and forming said first regions of said selection bipolar transistors; and

and a plurality of control contact regions of said second conductivity type and a second doping level, higher than said first doping level, formed in said active area regions and connected to biasing lines.

13. A cell array according to claim 12 wherein said bipolar transistor is of PNP type, said common region is a collector region, said second conduction regions are emitters of said bipolar transistors.

14. A cell array according to claim 13 wherein said active area regions are doped with arsenic and said first doping level of said active area regions (12; 42) is between $5*10^{17}$ and $5*10^{18}$ atoms/cm^3.

15. A cell array according to claim 13 wherein said body comprises a substrate extending below said common conduction region and having said first conductivity type and a third doping level, and a subcollector region extending between said substrate and said common conduction region, said subcollector region having said first conductivity type and a doping level higher than said common conduction region.

16. A cell array according to claim 15 wherein said subcollector region has a doping level comprised between 10^{18} and 10^{19} atoms/cm^3.

17. A cell array according to claim 15 wherein said common conduction region has a doping level comprised between 10^{17} and 10^{18} atoms/cm^3.

18. A cell array according to claim 12 wherein said second conduction regions have a doping level of about 10^{19}-10^{20} atoms/cm^3.

19. A cell array according to claim 12 wherein said storage component is a phase change memory element.

20. A memory device, comprising:

a storage component having first and second terminals; and

a selection bipolar transistor having a first conduction region, a second conduction region, and a base region, the first conduction region of the bipolar transistor being connected to the first terminal of the storage component, the bipolar transistor including:

a semiconductor body of a first conductivity type, forming the second conduction region of the bipolar transistor;

a first active region of a second conductivity type, overlying the semiconductor body and forming the base region of the bipolar transistor;

a first base contact region of the second conductivity type and a doping level that is higher than a doping level of the first active region, formed in the first active region and connected to a biasing line;

a first conduction region of the first conductivity type formed in, and surrounded by, the active region, the conduction region being spaced laterally apart from the base contact region by a first portion of the active region and forming the first region of the bipolar transistor; and

a first conductive contact positioned on the conduction region and connected between the conduction region and the storage component.

21. The memory device of claim 20 wherein the bipolar transistor and storage component comprise a first memory cell of a memory array of memory cells that includes a second memory cell having a second storage component and second bipolar transistor that includes:

a second active region of the second conductivity type, overlying the semiconductor body and forming a base region of the second bipolar transistor;

a second base contact region of the second conductivity type and a doping level that is higher than a doping level of the second active region, formed in the second active region and connected to the biasing line;

a second conduction region of the first conductivity type formed in, and surrounded by, the second active region, the second conduction region being spaced laterally apart from the second base contact region by a portion of the second active region and forming a first region of the second bipolar transistor; and

a second conductive contact positioned on the second conduction region and connected between the second conduction region and the second storage component.

22. The memory device of claim 21, further comprising a first field insulation region separating the first active region from the second active region.

23. The memory device of claim 22, further comprising:

a second field insulation region positioned on an opposite side of the first active region from the first field insulation region;

a third storage component; and

a third bipolar transistor that includes:

a third conduction region of the first conductivity type formed in, and surrounded by, the first active region, the second conduction region being spaced laterally apart from the first base contact region by a second portion of the first active region and forming a first region of the third bipolar transistor, the first and second portions of the first active region being positioned immediately adjacent to opposite sides of the first base contact region; and

a third conductive contact positioned on the third conduction region and connected between the third conduction region and the third storage component.

24. The memory device of claim 20 wherein the semiconductor body comprises:

a semiconductor substrate having the first conductivity type;

a common conduction region positioned immediately below the first active region and having the first conductivity type; and

a subcollector region extending between the substrate and the common conduction region, the subcollector region having the first conductivity type and a doping level higher than a doping level of the common conduction region.

25. The memory device of claim 24 wherein the subcollector region has a doping level comprised between 10^{18} and 10^{19} atoms/cm^3 and the common conduction region has a doping level comprised between 10^{17} and 10^{18} atoms/cm^3.

26. The memory device of claim 20 wherein the storage component is a phase change memory element.